

AMENDMENT & RESPONSE UNDER 37 C.F.R. § 1.116 - EXPEDITED PROCEDURE

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Dkt: 303.695US1

Serial Number: 09/598,355

Filing Date: June 21, 2000

Title: STRUCTURES AND METHODS FOR ENHANCING CAPACITORS IN INTEGRATED CIRCUITS

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wherein the morphology of the semiconductor structure remains stable when the trace amount of the first substance is oxidized during crystallization of the insulator layer.

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11. (Amended) A semiconductor structure for storing charges, comprising:
an insulator layer having a permittivity value greater than about 25; and
a [uniform] single conductive layer having a compound, wherein the compound remains stable when the insulator layer is crystallized at a high temperature so as to decrease the charge leakage of the insulator layer.

16. (Amended) A semiconductor structure for storing charges, comprising:
an insulator layer having a permittivity value; and
a [uniform] single conductive layer abuttingly coupled to the insulator layer and adapted to mitigate diffusion, wherein the crystalline structure of the insulator layer describes a desired lattice plane such that the permittivity value of the insulator layer is greater than about 25.

21. (Amended) A capacitor comprising:
a first electrode;
a dielectric that includes ditantalum pentaoxide; and
a second [uniform] single electrode having a compound that includes a first substance and a second substance, wherein the compound in an as-deposited state includes a substantial amount of the second substance so as to inhibit undesired diffusion at a high temperature, wherein the compound includes RuO_x, wherein the x is indicative of a desired number of atoms.

22. (Amended) A capacitor comprising:
a first electrode;
a dielectric that includes ditantalum pentaoxide; and
a second [uniform] single electrode having a compound that includes a first substance and a second substance, wherein the second electrode includes a trace amount of the first substance, wherein the morphology of the semiconductor structure remains stable when the trace amount of

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the first substance is oxidized during crystallization of the dielectric, wherein the compound includes RuO_x , wherein the x is indicative of a desired number of atoms.

23. (Amended) A capacitor comprising:
- a first electrode;
 - a dielectric that includes ditantalum pentaoxide; and
 - a second [uniform] single electrode having a compound, wherein the crystalline structure of the dielectric describes a (001) lattice plane, wherein the compound includes RuO_x , wherein the x is indicative of a desired number of atoms.
24. (Amended) A capacitor comprising:
- a first electrode;
 - a dielectric having a first compound that includes a first substance and a second substance, wherein the first compound includes ditantalum pentaoxide; and
 - a second [uniform] single electrode having a second compound that includes a third substance and a fourth substance, wherein the second electrode includes a trace amount of the third substance, wherein the second compound in an as-deposited state includes a substantial amount of the fourth substance, wherein the trace amount of the third substance is oxidized during the crystallization of the dielectric such that a diffusion of at least one of the first substance and the second substance is inhibited, wherein the crystalline structure of the dielectric describes substantially a (001) lattice plane, and wherein the second compound includes RuO_x , wherein the x is indicative of a desired number of atoms.
25. (Amended) A capacitor comprising:
- a first electrode having a substance that is selected from a group consisting of TiN, TiON, WN_x , TaN, Ta, Pt, Pt-Rh, Pt-RhO_x, Ru, RuO_x, Ir, IrO_x, Pt-Ru, Pt-RuO_x, Pt-Ir, Pt-IrO_x, SrRuO₃, Au, Pd, Al, Mo, Ag, and Poly-Si;
 - a dielectric having a first compound that includes a first substance and a second substance, wherein the first compound includes ditantalum pentaoxide; and

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a second [uniform] single electrode having a second compound that includes a third substance and a fourth substance, wherein the second electrode includes a trace amount of the third substance, wherein the second compound in an as-deposited state includes a substantial amount of the fourth substance, wherein the trace amount of the third substance is oxidized during the crystallization of the dielectric such that a diffusion of at least one of the first substance and the second substance is inhibited, wherein the crystalline structure of the dielectric describes substantially a (001) lattice plane, and wherein the second compound includes RuO_x , wherein the x is indicative of a desired number of atoms.

51. (Amended) A memory device comprising:

an array of memory cells, wherein the array includes at least one capacitor that includes:

an insulator layer having a first compound that includes substances;

a [uniform] single conductive layer having a second compound that includes a first substance and a second substance, wherein the second compound in an as-deposited state includes a substantial amount of the second substance so as to inhibit undesired diffusion of at least one substance of the first compound from the insulator layer;

an address decoder;

a row access circuitry;

a column access circuitry;

a controller; and

an input/output circuit.

52. (Amended) An electronic system comprising:

a plurality of circuit modules includes a plurality of dies, wherein at least one die includes at least one array of memory cells, wherein the array comprises at least one capacitor that includes:

an insulator layer having a first compound that includes substances;

a [uniform] single conductive layer having a second compound that includes a first substance and a second substance, wherein the second compound in an as-deposited state

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includes a substantial amount of the second substance so as to inhibit undesired diffusion of at least one substance of the first compound from the insulator layer;

at least one transistor having a gate, drain, and source, wherein the drain is coupled to the second conductive layer;

a plurality of leads coupled to the plurality of dies to provide unilateral or bilateral communication and control; and

a user interface.

53. (Amended) A computer system comprising:

a processor;

a memory system that comprises a plurality of memory modules, wherein one of the plurality of memory modules comprises a plurality of memory devices, wherein at least one memory device comprises at least one array of memory cells, wherein the array comprises at least one capacitor that includes:

an insulator layer having a first compound that includes substances;

a [uniform] single conductive layer having a second compound that includes a first substance and a second substance, wherein the second compound in an as-deposited state includes a substantial amount of the second substance so as to inhibit undesired diffusion of at least one substance of the first compound from the insulator layer; and

at least one transistor having a gate, drain, and source, wherein the drain is coupled to the second conductive layer;

a plurality of command links coupled to the plurality of memory devices to communicate at least one command signal;

a plurality of data links coupled to the plurality of memory devices to communicate data;

a memory controller;

at least one user interface device, wherein the at least one user interface device includes a monitor;

at least one output device, wherein the at least one output device includes a printer; and

at least one bulk storage device.